

HAFIZA KART TEST SONUÇLARI / FARKLI MARKA SD KARTLAR İLE KARŞILAŞTIRILMASI

TEST YAPILAN PC ÖZELLİKLERİ

Anakart : ASUS B450M-KII

İşlemci : AMD RYZEN 3 1200

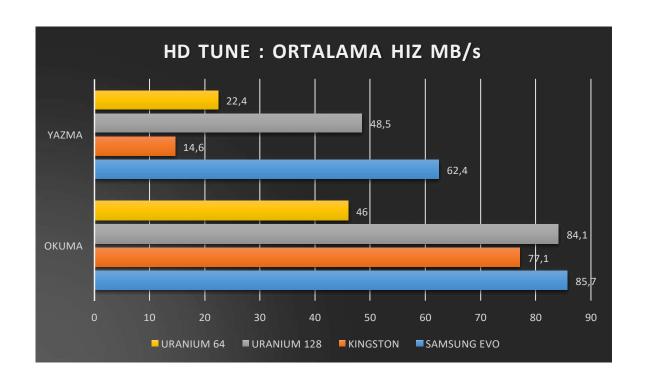
RAM : GOODRAM IRP-K3600D4V64L 18S/8G (8 gb)

Ekeran Kartı : SECLIFE GT610 2G D3 64BIT

İşletim Sistemi : WINDOWS 10 64 BIT

EK Donanim : TRUST 21935 KART OKUYUCU

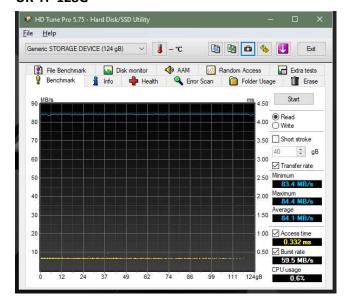
Uygulamalar : HD Tune Pro 5,75 / Crystal Disk Mark 8.0.4 / h2testw

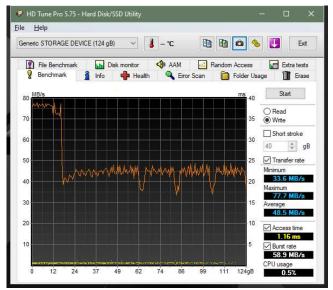


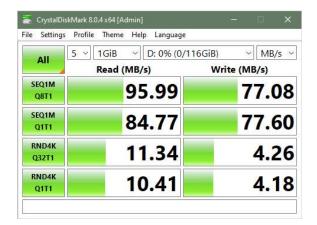
 Gerçekçi ve doğru sonuçları HD TUNE uygulaması olduğu düşünüldüğünden sadece bu uygulamanın sonuçları grafiklendirilmiştir.

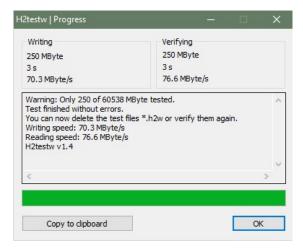
Aşağıda her kart için HD TUNE dahil farklı uygulamalar ile yapılan test sonuçları verilmiştir.

UR-TF-128G

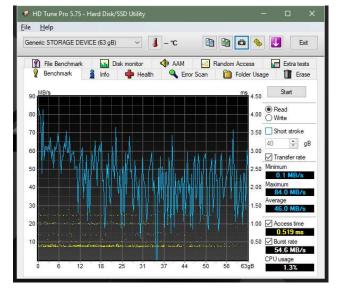


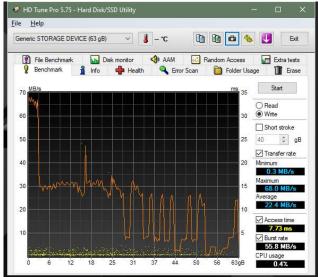


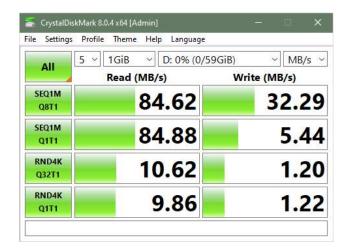


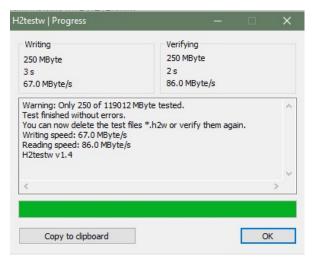


UR-TF-64G

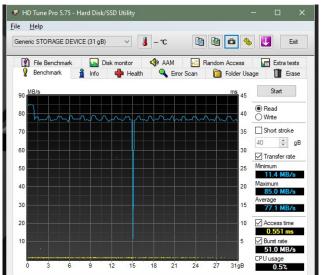


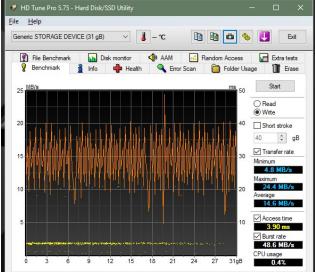


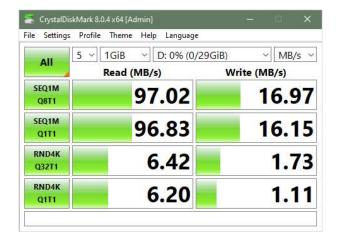


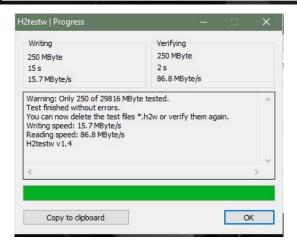


KINGSTON CANVAS Select Plus 32gb U1

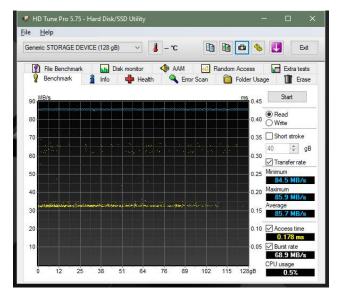


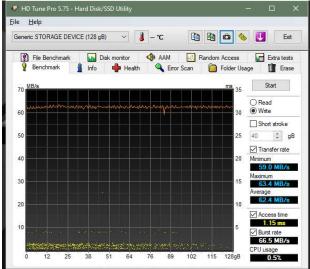


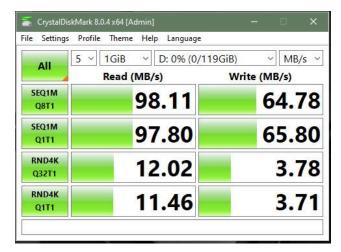


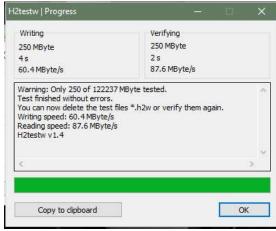


SAMSUNG EVO PLUS U3











INDUSTRIAL HAFIZA KARTI DATASHEET

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Description

microSD3.0 card series are non-volatile, which means no external power is required to retain the information stored on it. The microSD3.0 Cards are fully compatible with Physical Layer Specification, Version 3.0 (this specification is available from the SDA), support Ultra High Speed (UHS), provides high write/read speed and high IOPS, it was designed to meet the security, high capacity, high performance and environmental requirements inherent in next generation consumer electronic devices. The SD card system is a new mass-storage system based on innovations in semiconductor technology. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. SD card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors consumer electronic device.

Ultra High Speed (UHS) Card
It provides up to 104MB/s* performance.
UHS cards are backward compatible on non-UHS hosts.
*Based on internal testing; performance may vary depending upon host device.
1 megabyte (MB)=1,000,000byte

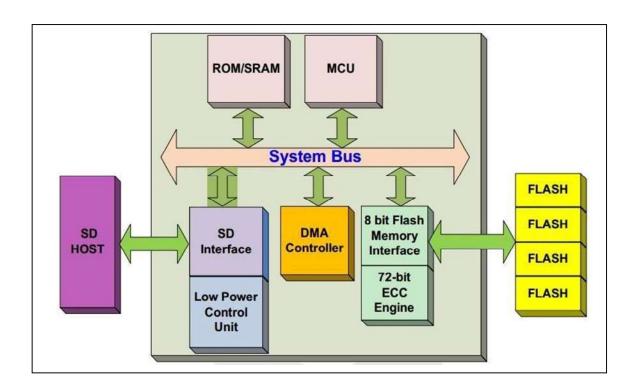


2 Features

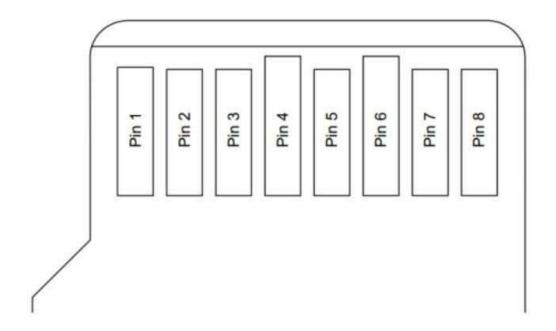
- ROHS compliant product.
- Capacity:
- Standard Capacity SD Memory Card (SDSC): Up to and including 2GB
- ▶ High Capacity SD Memory Card (SDHC): More than 2GB and up to and including 32GB
- Extended Capacity SD Memory Card (SDXC): More than 32GB and up to and including 2TB
- Complies to SD specifications version 3.0.
- Supports dual voltage 3.3V and 1.8V host interface power supply.
- Comply with SD Association File System Specification.
- Targeted for portable and stationary applications.
- Greater Performance Choices.
- Bus Speed Mode:
- DS-Default Speed mode: 3.3V signaling, frequency up to 25MHz, up to 12.5MB/sec
- ➤ HS-High Speed mode: 3.3V signaling, frequency up to 50MHz, up to 25MB/sec
- > SDR12-1.8V signaling, frequency up to 25MHz, up to 12.5MB/sec
- > SDR25-1.8V signaling, frequency up to 50MHz, up to 25MB/sec
- SDR50-1.8V signaling, frequency up to 100MHz, up to 50MB/sec
- SDR104-1.8V signaling, frequency up to 208MHz, up to 104MB/sec
- DDR50 1.8V signaling, frequency up to 50 MHz, up to 50MB/s.
- Switch function command supports Bus Speed Mode, Command System, Drive Strength, and future functions.
- Content Protection Mechanism Complies with highest security of SDMI standard.
- Built-in write protection features (permanent and temporary)
- Password protection (CMD42-LOCK_UNLOCK).
- Sophisticated system for error recovery including a powerful ECC.
- Global Wear Leveling.
- Weight: SD Card Max. 2.5g / microSD Card Max. 1g
- Dynamic Power Management Technology
- Quick standby, auto-suspend, and sleepoperations.
- Sleep current: about 100uA



3 Block Diagram



4 Pin Assignment





4.1 Pin Definition

Pin No.	SD Mode		SPI Mode			
	Name	Туре	Description	Name	Туре	Description
1	DAT2	I/O/PP	Data Line [Bit2]	RSV		Reserved
2	CD/DAT3	I/O/PP	Card Detect / Data Line [Bit3]	cs	l	Chip Select
3	CMD	PP	Command / Response	DI	l	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		Reserved

S: Power Supply;

I: Input;O: Output;

PP: Push-Pull



5 Product Info

5.1 Product list

Capacity	File System	Speed Class	Endurance (P/E cycles)
4GB	FAT32	⊍√10	10000
8GB	FAT32	⊕V10	10000
16GB	FAT32	⊍V10	10000
32GB	FAT32	⊍√ 30	1000
64GB	exFAT	⊍ ∨ 30	1000
128GB	exFAT	⊍ ∨ 30	1000
256GB	exFAT	⊍√ 30	1000
512GB	exFAT	⊍ ∨ 30	1000

Note:

Measurement based on VTE3100 & VTE4100 TestMetrix device, SW 3.2A software or up version. The card must be reformatted between each script test. Test scripts:

SD_Card(Spec3.0_High&Extended-Capacity_UHS-I and Non-UHS-I)_Compliance [rev32A]-B87.vte SD_Card (Spec2.0-3.0 High&Extended-Capacity_UHS-I) Performance-Speed (Multiple Block Sequential) [rev31M] - SDR104-With Background Data.vte;

SD_Card (Spec3.0-4.0 HC & XC -UHS-I) SD 3.0 Speed Class (Grade 1/3) [rev32A].vte SD [Spec 5.1_HC&XC_UHS-I] Speed Class (Grade 1) & VSC_6_10_30 [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.2-52B-A05].vte

SD [Spec 5.1_HC&XC_UHS-I] A1 Test - SDR50 (w CMD12_DB) [VTE4100, Rail_UHS-I+II] SK1 [5.2.0.1-52A-A00].vte



6 Reliability and durability

6.1 Absolute Maximum Temperature Rating

[Table 11]: Maximum Temperature Rating

Item	Symbol	Parameter	MIN	MAX
1	Та	Operating Temperature	0°C	+70°C
2	Tst	Storage Temperature	-40°C	+85°C

6.2 Supply Voltage Range

[Table 12]: Supply voltage range

Item	Symbol	Parameter	MIN	MAX
1	VDD	Operating Voltage Support	+2.7V	+3.6V
2	VSS	GND	-0.3V	+0.3V

6.3 Temperature Range and Humidity

[Table 13]: High Temperature

Parameter	Temperature	Humidity
Operation	+70°C	0% RH
Storage	+85°C	0% RH

[Table 14]: Low Temperature

Parameter	Temperature	Humidity
Operation	0°C	0% RH
Storage	-40°C	0% RH

[Table 15]: Temperature Cycle

Parameter	Temperature Range
Operation	0°C~ +70°C
Storage	-40°C~ +85°C

[Table 16]: High Humidity

Parameter	Temperature	Humidity
Operation	+25°C	93% RH
Storage	+40°C	93% RH

6.4 Shock



[Table 20]: Shock

	Condition
Shock Test	200G (1961.33m/sec2) 3ms ,150G (1471.00m/sec2) 10ms From X.Y. Z, 3 directions/ 3 times each

6.5 Vibration

[Table 21]: Vibration

	Condition	Vibration Orientation
Vibration Test	10 ~ 2000Hz, 6Grms	X, Y, Z axis/30 min for each

6.6 Drop Test

[Table 22]: Drop

	Condition
Drop Test	1.5[m] free fall

6.7 Bending

[Table 23]: Bending

	Condition
Bending Test	10[N] Center 200[mm/minute] 60[sec]

6.8 Torque

[Table 24]: Torque

	Condition
Torque Test	0.15[Nm] +/- 2.5[deg] max. 30[sec]

6.9 Electrostatic Discharge (ESD)

[Table 25]: Drop Specification

	Condition
ESD Test	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF], 330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]

7 SD CARD COMPARISON



[Table 26]: Comparing SDSC, SDHC and SDXC

abic 20] . Companing obco,	02110 0110 02710		
	SDSC (Backward compatible to 2.0 host)	SDHC (Backward compatible to 2.0 host)	SDXC
File System	FAT 12/16	FAT32	exFAT
Addressing Mode	Byte (1 byte unit)	Block (512 byte unit)	Block (512 byte unit)
HCS/CCS bits of ACMD41	Support	Support	Support
CMD8 (SEND_IF_COND)	Support	Support	Support
CMD16 (SET_BLOCKLEN)	Support	Support (Only CMD42)	Support (Only CMD42)
Partial Read	Support	Not Support	Not Support
Lock/Unlock Function	Mandatory	Mandatory	Mandatory
Write Protect Groups	Optional	Not Support	Not Support
Supply Voltage 2.7v - 3.6v (for operation)	Support	Support	Support
Total Bus Capacitance for each signal line	40pF	40pF	40pF
CSD Version (CSD_STRUCTURE Value)	1.0 (0x0)	2.0 (0x1)	2.0 (0x1)
Speed Class	Optional	Mandatory (Class 2 / 4 / 6 / 10)	Mandatory (Class 2 / 4 / 6 / 10)

[Table 27]: Comparing UHS Speed Grade Symbols

	inpaining of the operation and a contraction	
	U1 (UHS Speed Grade 1)	U3 (UHS Speed Grade 3)
Bus Mode	UHS-I /UHS-II	
SD Memory Card	SDHC, SDXC	
Mark	ប	3
Performance	10 MB/s minimum write speed	30 MB/s minimum write speed
Applications	Full higher potential of recording realtime broadcasts and capturing large-size HD videos.	Capable of recording 4K2K video.

[Table 28] : Comparing Video Speed Class Symbols

V6 (Video Speed Class 6) V10 (Video Speed Class 10)	V30 (Video	V60 (Video	V90 (Video
	Speed Class 30)	Speed Class 60)	Speed Class 90)



Bus Mode	High Speed/UHS-I/UHS-II		UHS-I/UHS-II	UHS-II		
SD Memory Card	SDHC, SDXC					
Mark	V 6	orV	V 30	V 60	V 90	
Performanc e	6 MB/s minimum write speed	10 MB/s minimum write speed	30 MB/s minimum write speed	60 MB/s minimum write speed	90 MB/s minimum write speed	
Applications	HD/FHD Video Recording.	FHD Video Recording HD Still Image Continuous Shooting.		4K/2K Video Recording	8K/3D/360° Video Recording	

[Table 29]: Comparing Application Performance Class Symbols

	A1 (Application Performance Class 1)	A2 (Application Performance Class 2)			
Mark	<i>A</i> 1	<i>A</i> 2			
Min. Random Read	1500 IOP	4000 IOPS			
Min. Random Write	500 IOPS	2000 IOPS			
Min. Sustained Sequential Write	10 MB/s	10 MB/s			
Applications	Main target is uSD for Android mobile handset				

Note: 1) IOPS means Input/Output Operations Per Second.



8 Bus Operating Conditions

8.1 General

Parameter	Symbol	Min.	Max.	Unit	Remark		
Peak voltage on all lines		-0.3	3.6	V			
All Inputs							
Input Leakage Current		-10	10	μΑ			
All Outputs							
Output Leakage Current		-10	10	μΑ			

8.2 Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	VDD	2.75	3.6	V	CMD0, 15,55, ACMD41 commands
Supply voltage specified in OCR register					Except CMD0, 15,55, ACMD41 commands
Supply voltage differentials (VSS1, VSS2)		-0.5	0.5	V	
Power up time			250	ms	From 0v to VDD Min.

Note. The current consumption of any card during the power-up procedure must not exceed 10 mA



8.3 Bus Signal Line Load

The total capacitance CL the CLK line of the SD Memory Card bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line:

Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:

Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	CL		10	pF	fPP ≤ 20 MHz, 7 cards
Single card capacitance	CCARD		10	pF	
Maximum signal line inductance			16	nH	fPP ≤ 20 MHz
Pull-up resistance inside card (pin1)	RDAT3	10	90	ΚΩ	May be used for card detection

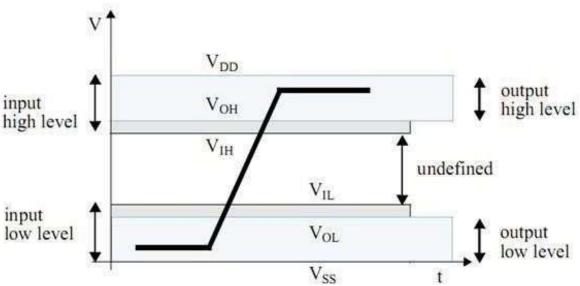
Note that the total capacitance of CMD and DATA lines will be consisted of CHOST, CBUS and one CCARD only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull up resistance for SD command line	RCMD	10	100	ΚΩ	
Pull up resistance for SD data line	RDAT	10	100	ΚΩ	To prevent bus floating
Bus signal line capacitance	CL		250	pF	fPP ≤ 5 MHz, 21 cards



9 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

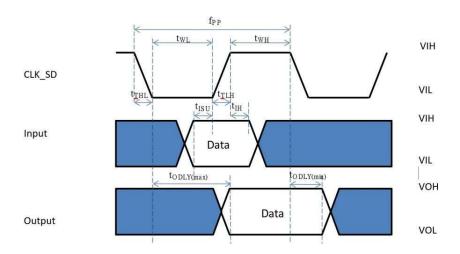


To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any VDD of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	VOH	2.4		V	
Output LOW voltage	VOL		0.4	V	
Input HIGH voltage	VIH	2.0	3.6	V	
Input LOW voltage	VIL	VSS -0.3	0.8	V	



10 Bus Timing



Parameter	Symbol	Min	Max.	Unit	Remark	
Input CLK_SD						
Clock frequency data transfer mode	fPP	-	50	MHz	CL ≦ 10pF (1 card)	
Clock frequency identification mode	fOD	-	400	KHz	CL ≦ 10pF (1 card)	
Clock low time / Clock high time	tWL/tWH	7	-	ns	CL ≦ 10pF (1 card)	
Clock rise time / Clock fall time	tTLH/tTHL	-	3	ns	CL ≦ 10pF (1 card)	
Input CMD_SD/DATA_SD, reference to CLK	SD		1	1		
Input set-up time	tISU	6	-	ns	CL ≦ 10pF (1 card)	
Input hold time	tIH	2	-	ns	CL ≦ 10pF (1 card)	
Output CMD_SD/DATA_SD, reference to CL	.K_SD					
Output delay time during Data Transfer Mode	tODLY	-	14	ns	CL ≦ 40pF (1 card)	
Output delay time during Identification Mode	tODLY	-	50	ns	CL ≦ 40pF (1 card)	
Inputs CMD, DAT (referenced to CLK)		1				
Input set-up time	tISU	5		ns	CL ≤ 25 pF, (1 cards)	
Input hold time	tIH	5		ns	CL ≤ 25 pF, (1 cards)	
Outputs CMD, DAT (referenced to CLK)						
Output Delay time	tODLY	0		ns	CL ≤ 25 pF, (1 cards)	



11 Register Information

Within the card interface six registers are defined: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.

Register Name	SD 3.01	SD 2.02	SD 1.1	SD 1.01
Operation Condition Register (OCR)	V	V	V	V
Card Identification Register (CID)	V	V	V	V
Driver Stage Register (DSR)	V	V	V	V
Relative Card Address Register (RCA)	V	V	V	V
Card Specific Data Register (CSD)	V	V	V	V
SD card Configuration Register (SCR)	V	V	V	V

11.1 OCR register

The 32-bit operation conditions register stores the VDD voltage profile of the card. In addition, this register includes a status information bit. This status bit is set if the card power up procedure has been finished. The OCR register shall be implemented by the cards which do not support the full operating voltage range of the SD Memory Card bus, or if the card power up extends the definition in the timing diagram.

OCR bit	VDD voltage window	High voltage SD	Dual voltage SD
[6:0]	Reserved	000 0000 b	000 0000 ь
[7]	1.7V~1.95V	0 b	1 b
[14:8]	2.0V - 2.6V	000 0000 b	000 0000 ь
[23:15]	2.7V - 3.6V	1 1111 1111 b	1 1111 1111 b
[24]	Switch to 1.8V Accepted		
[29:25]	Reserved	00 0000 b	00 0000 ь
[30]	Card capacity status		
[31]	Card power up status bit		

A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.



11.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

CID bit	Width	Name	Field	Value
[127:120]	8	Manufacture ID	MID	
[119:104]	16	OEM/Application ID	OID	
[103:64]	40	Product Name	PNM	
[63:56]	8	Product Revision	PRV	
[55:24]	32	Product Serial Number	PSN	
[23:20]	4	Reserved	-	
[19:8]	12	Manufacturing Date	MDT	
[7:1]	7	CRC7 check sum	CRC	
[0]	1	Not used, always '1'	-	

11.3 CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows: R= readable, W(1) = writable once, W = multiple writable.



CSD bit	Width	Name	Field	Value	Note
[127:126]	2	CSD structure	CSD_STRUCTURE	01b	v2.0 (High Capacity and Extended Capacity)
[125:120]	6	Reserved	-	-	-
[119:112]	8	Data read access-time 1	TAAC	0Eh	1 ms (*3)
[111:104]	8	Data read access-time 2	NSAC	00h	(*3)
[103:96]	8	Max. data transfer rate	TRAN_SPEED	32h	25 MHz
[95:84]	12	Card command classes	ccc	5F5h	(*1)
[83:80]	4	Max. read data block length	READ_BL_LEN	9h	512 bytes(*3)
[79]	1	Partial block read allowed	READ_BL_PARTIAL	0b	Not Support (*3)
[78]	1	Write block misalignment	WRITE_BLK_MISALIGN	0b	Not Support (*3)
[77]	1	Read block misalignment	READ_BLK_MISALIGN	0b	Not Support (*3)
[76]	1	DSR implemented	DSR_IMP	0b	Not support
[75:70]	6	Reserved	-	00h	-
[69:48]	22	Device size	C_SIZE	(*2)	(*2)
[47]	1	Reserved	-	0	-
[46]	1	Erase single block enable	ERASE_BLK_EN	1b	allowed(*3)
[45:39]	7	Erase sector size	SECTOR_SIZE	7Fh	64KB(*3)
[38:32]	7	Write protect group size	WP_GRP_SIZE	00h	(*3)
[31]	1	Write protect group enable	WP_GRP_ENABLE	0b	Not Support(*3)
[30:29]	2	Reserved	-	-	-
[28:26]	3	Write speed factor	R2W_FACTOR	010b	4X(*3)
[25:22]	4	Max. write data block length	WRITE_BL_LEN	9h	512 bytes(*3)
[21]	1	Partial block writes allowed	WRITE_BL_PARTIAL	0b	Not Support(*3)
[20:16]	5	Reserved	-	-	-
[15]	1	File format group	FILE_FORMAT_GRP	0b	HD like FAT(*3)
[14]	1	Copy flag	COPY	0b	Not copied
[13]	1	Permanent write protection	PERM_WRITE_PROTECT	0 b	Not protected
[12]	1	Temporary write protection	TMP_WRITE_PROTECT	0 b	Not protected
[11:10]	2	File format	FILE_FORMAT	00 b	HD like FAT(*3)
[9:8]	2	ECC code	ECC	00 b	None
[7:1]	7	CRC	CRC	-	-
[0]	1	Not used, always '1'	-	1 b	-

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.



11.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value0x0000 is reserved to set all cards into the Stand-by State with CMD7.

11.5 DSR Register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

11.6 SCR Register

In addition to the CSD register there is another configuration register that named - SD CARD Configuration Register (SCR). SCR provides information on SD Memory Card's special features that were configured into the given card. The size of SCR register is 64bit. This register shall be set in the factory by the SD Memory Card manufacturer. The following table describes the SCR register content.



SCR bit	Width	Name	Field	Value	Note
[63:60]	4	SCR structure	SCR_STRUCTURE	0000 ь	v1.0-v3.01
[59:56]	4	SD card spec. version	SD_SPEC	0010 b	V2.0 or V3.0X
[55]	1	Data status after erase	DATA_STAT_AFTER_ ERASE	0 b	Zero after erase
				010 b	SDSC Card
[54:52]	3	CPRM Security Speciation	SD SECURITY	011 b	SDHC Card
[04.02]	[54.52]	Version	0D_0E0011111	100 b	SDXC Card
[51:48]	4	DAT bus width support	SD_BUS_WIDTH	0101 b	Support 1/4 bit
[47]	1	Spec. Version 3.00 or higher	SD_SPEC3	1 b	V3.0X
[46:43]	4	Extended Security Support	EX_SECURITY	0000 ь	Support extended security
[42:34]	9	Reserved	-	-	-
			CMD23_SUPPORT	0 b/1 B	SDR[33] mandatory for UHS104 card
[33:32]	2	Command Support bits	CMD20_SUPPORT	0 b/1 B	SDR[32] mandatory for SDXC card
[31:0]	32	Reserved	-	-	-



11.7 SD Status Register

The SD Status contains status bits that are related to the SD Memory Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran_state' (card is selected). SD Status structure is described in below. Unused reserved bits shall be set to 0

[Table 10]: SD Status Register

Bits	Identifier	Туре	Value	Description
511:510	DATA_BUS_WIDTH	SR	'00'=1(default) '01'=reserved '10'=4 bit width '11'=reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command
509	SECURED_MODE	SR	'0'=Not in the mode '1'=In Secured Mode	Shows if the card is in the secured mode of operation or not. (refer to "Part 3 Security Specification").
508:502	Reserved for Security Functions (Refer to Part 3 Security Specification)			
501:496	Reserved			
495:480	SD_CARD_TYPE	SR	'00xxh'=SD Memory Cards ('x'=don't care). The following cards are currently defined: '0000h'=Regular SD RD/WR Card. '0001h'=SD ROM Card '0002h'=OTP	In the future, the 8 LSBs will be used to define different variations of an SD Memory Card(Each bit will define different SD Types)
479:448	SIZE_OF_PROTECTED_AREA	SR	Size of protected area	(See section 4.10.2.1)
447:440	SPEED_CLASS	SR	Speed Class of card	(See section 4.10.2.2)
439:432	PERFORMANCE_MOVE	SR	Performance of move indicated by 1[MB/s] step.	(See section 4.10.2.3)

431:428	AU_SIZE	SR	Size of AU	(See section 4.10.2.4)
427:424	Reserved			
423:408	ERASE_SIZE	SR	Number of AUs to be erased at a time	(See section 4.10.2.5)



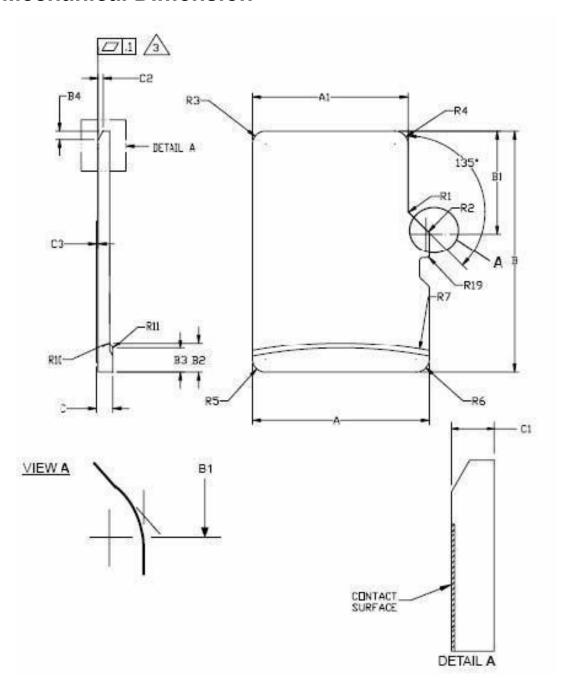
				· · · · · · · · · · · · · · · · · · ·
407:402	ERASE_TIMEOUT	SR	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See section 4.10.2.6)
401:400	ERASE_OFFSET	SR	Fixed offset value added to erase time	(See section 4.10.2.7)
399:396	UHS_SPEED_GRADE	SR	Speed Grade for UHS mode	(See section 4.10.2.8)
395:392	UHS_AU_SIZE	SR	Size of AU for UHS mode	(See section 4.10.2.9)
391:384	VIDEO_SPEED_CLASS	SR	Video Speed Class value of the card	(See section 4.10.2.10)
383:378	reserved			
377:368	VSC_AU_SIZE	SR	AU size in MB for Video Speed Class	(See section 4.10.2.11)
367:346	SUS_ADDR	SR	Suspension Address	(See section 4.10.2.12)
345:340	reserved			
339:336	APP_PERF_CLASS	SR	Application Performance Class Value of the card	(See section 4.10.2.13)
335:328	PERFORMANCE_ENHANCE	SR	Support for Performance Enhancement functionalities	(See section 4.10.2.14)
327:314	reserved			
313	DISCARD_SUPPORT	SR	'0' Not Supported '1' Supported	Discard Support. (See section 4.3.6)
312	FULE_SUPPORT	SR	'0' Not Supported '1' Supported	Full User Area Logical Erase Support. (See section 4.3.7)
311:0	Reserved for Manufacturer			

11.8 SPI Mode Card Registers

Unlike the SD Memory card protocol (where the register contents is sent as command response), reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by data block of 16 bytes suffixed with a 16bit CRC. The data timeout for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore, the standard response timeout value(NCR) is used for read latency of the CSD register.

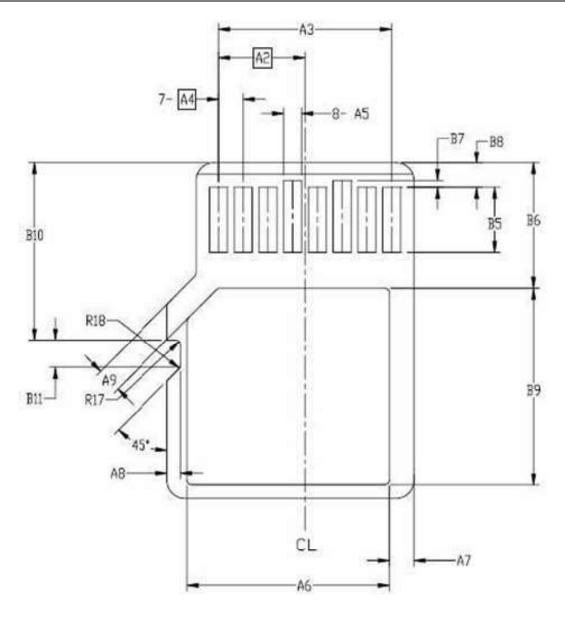


12 Mechanical Dimension



Mechanical Description: Top View





Mechanical Description: Bottom View



	COMMON	DIMENS	IONS	
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1.	9.60	9.70	9.80	L Sellings
A2		3,85		BASIC
A3	7.60	7.70	7.80	
A4		1.10		BASIC
A5	0.75	0.80	0.85	
AB			8.50	
A7	0.90			
A8	0.60	0.70	0.80	
A9	0.80			
В	14.90	15.00	15.10	
B1	6.30	6.40	8.50	
B2	1.64	1.84	2.04	
B3	1,30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50			
B7	0.20	0.30	0.40	
B8	1.00	1.10	1,20	
80	-		9.00	
810	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
С	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00		0.15	
D1	1.00		-	
D2	1.00			
D3	1.00		-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
RO	0.70	0.80	0.80	
R7	29.50	30.00	30.50	
R10	-	0.20		
R11		0.20	*	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	

Notes:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 2. DIMENSIONS ARE IN MILLIMETERS.
- COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

microSD package: Dimensions